Irradiation Study on GEM IPC Preamp/Shaper

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1. Overview of the Integrated Circuit:

The Preamplifier/Shaper Integrated Circuit for the **GEM**Interpolating Pad Chamber (IPC), designed by Paul. O' Connor, Brookhaven National
Laboratory is for amplifying the charge signal from the Pad cathodes into a voltage pulse
which goes to the Analog Random Access Memory (ARAM) integrated circuit. The GEM
IPC integrated circuit has a SemiGaussian voltage pulse output with a 30ns shaping time.
The integrated circuits were fabricated using Harris Semiconductors AVLSI1-RA process
in-order for the electronics on the wafer to survive up to 2 Mrad of ionizing radiation
during its operation life time. The details of the electronics on the GEM IPC integrated
circuits is explained in the design memorandum ¹ by Paul. O' Connor.

The purpose of this study is to determine the ability of the electronics on this IC fabricated using the above process to withstand ionizing radiation up to the above mentioned dose level.

2. About the Process:

Foundry services for the GEM IPC integrated circuits were provided by Harris Semiconductor Corporation.

The process used for fabricating the GEM IPC integrated circuits was **AVLSI1-RA**, which is a **R**adiation Hardened - **A**nalog process. This process is a P-tub process with substrate being N+. The Gate Oxide thickness is 250 angstrom of wet oxide. Many process parameters and process description are not discussed here since they are proprietary information of Harris Semiconductor Corporation.

3. Irradiation and Measurement setup:

The GEM IPC integrated circuits were irradiated using 60 Co source at the Solid State Gamma Irradiation Facility, BNL. The IC's were irradiated under identical operating conditions (power, biasing) to that of the measurement setup on the test bench. The test structure consisted of the channel 0 shaper output fed to an emitter follower configured to drive 50 ohm scope termination through a 10uF blocking capacitor. co-axial connectors were used. Lecroy 7200 scope was used for Noise measurements and Tektronix DSA 602 was used for gain, linearity and shaping time measurements. The test transistors were tested for its DC behavior using HP 4145 semiconductor parameter analyzer. The transistors were biased as follows:

The gate voltages of both large and small mosfets had to be the same since they were connected together on chip.

The preamp/shaper section was biased similarly to that of the test board with external resistors for current mirror load. The following tests were done on the electronics on the chip.

- Preamp/Shaper chain gain, linearity, shaping time and noise.
- DC characteristics on the test transistors.

The integrated circuits were irradiated in the following steps.

0.5 Mrad, 1.0 Mrad, 2.0 Mrad, 5.0 Mrad, 10.0 Mrad and 50.0 Mrad

The above figures are total dose administered to the GEM IPC integrated circuits. The devices were exposed to radiation at the dose rates of $3.1x10^4$ rad/hr, $3.1x10^4$ rad/hr, $6.2x10^4$ rad/hr, $1.7x10^5$ rad/hr, $5.3x10^4$ rad/hr and $3.6x10^4$ rad/hr to achieve the total dose of 0.5 Mrad, 1.0 Mrad, 2.0 Mrad, 5.0 Mrad, 10.0 Mrad and 50.0 Mrad respectively. The electronics were tested immediately after the radiation and were subjected to radiation within 4 hours.

4. Results on Test Transistors:

The variation of the threshold of both Nmos and Pmos are shown in fig. 1 and 2.

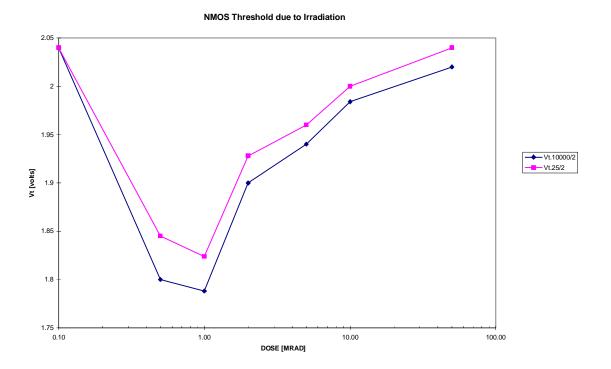


Fig. 1

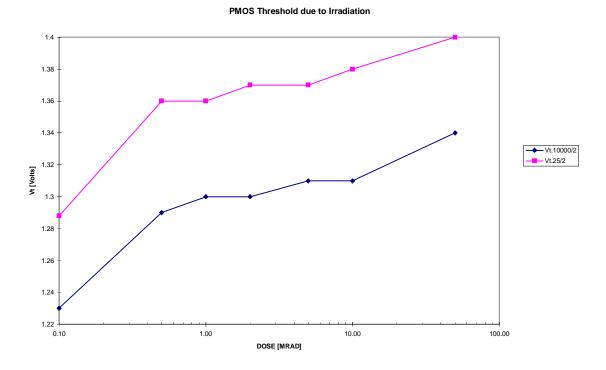


Fig. 2

Due to the different rates of buildup of fast states and oxide trapped holes the well known phenomenon of "Turnaround" effect is seen only in the N-channel mosfet and not in the P-channel mosfet as explained by Freeman and Holmes Siedle ². It is also observed that the VTNZ effect, (which is 'Vt of the N-channel mosfet crossing zero' leading to a large increase of quiescent current) is not seen on the test transistors. This effect plays a leading role in failure of most electronics on radiation. Also the threshold shift in the P-channel mosfet is appreciably smaller as expected and explained by many others who have worked in the study of CMOS devices due to radiation. The Id-Vgs, Id-Vds and Gm-Id curves for the test transistors are shown in the following graphs.

Id-Vgs curves for the nmos 10000/2 and 25/2 transistors are shown in Fig. 3 and Fig. 4 respectively. The effect of "Turnaround" can be seen evidently from this curves and also it can be seen that the transistors were in the verge of "Super-Recovery" or "Rebound" which is the threshold overshooting the pre-radiated threshold value as explained by Andrew Holmes-Siedle and Len Adams ².

NMOS 10000/2 Id-Vgs due to Irradiation

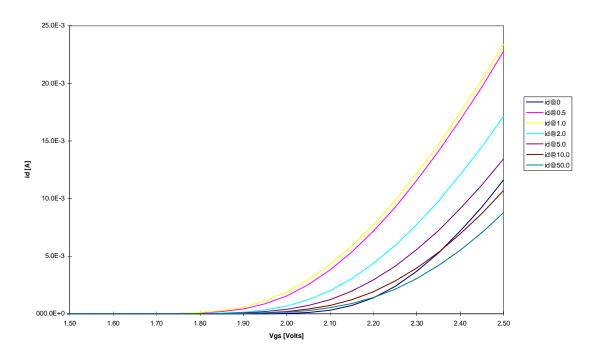


Fig. 3

PMOS 10000/2 Id- Vgs due to Irradiation

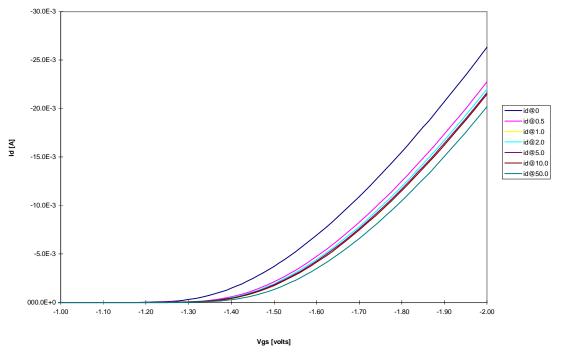


Fig. 4

The Id-Vgs curves for the pmos transistors are given and it is observed as expected that the threshold voltage is disrupted by a small amount on the first step of irradiation and after that no appreciable change in the threshold is seen, as seen in that of nmos.

The Gm -Id curves for the large (W/L ratio of 10000/2) p-channel and n-channel mosfets are shown in Fig. 5 and Fig. 6.

Gm [nmos:10000/2] due to Irradiation

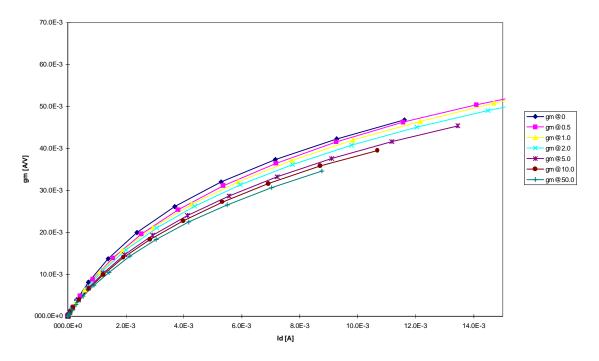


Fig. 5

Gm [pmos:10000/2]

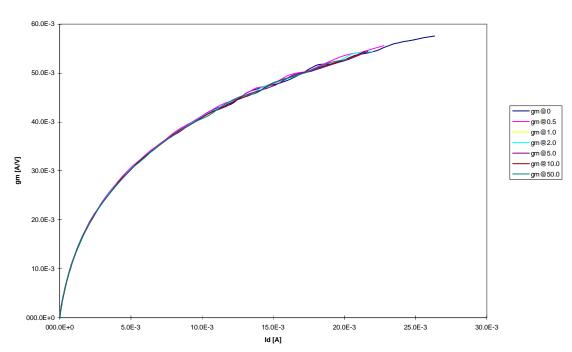


Fig. 6

The gm of the two large transistors at 4 ma are shown in fig 7 and fig 8 .

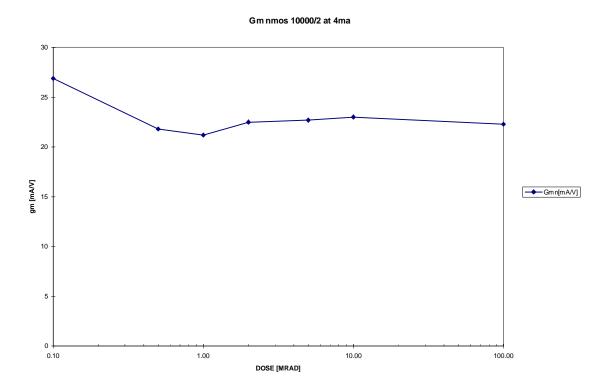


Fig. 7

Gm pmos 10000/2 at 4ma

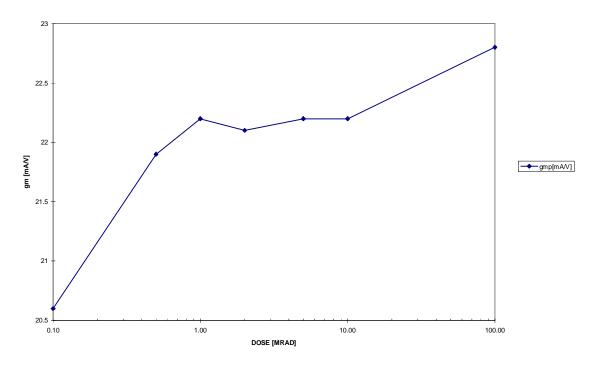


Fig. 8

The subthreshold region current curves for both the large n-channel and p-channel mosfets are shown in the following two figures Fig. 9 and Fig. 10 respectively.



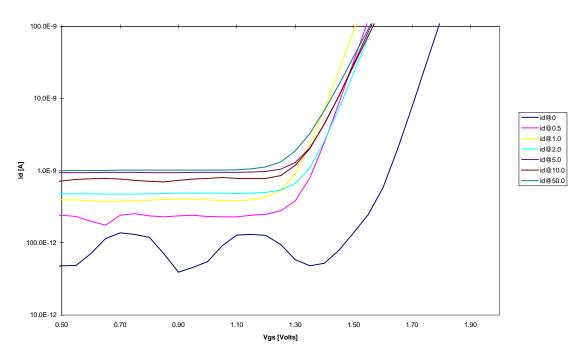


Fig. 9

PMOS 10000/2 Subthreshold current curves

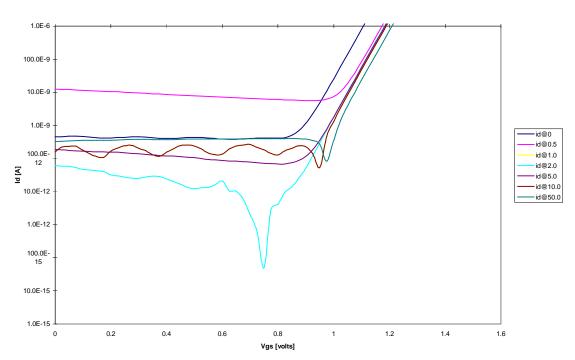


Fig. 10

The leakage current at various dose levels are given in Fig. 11 and Fig. 12.

NMOS [10000/2] leakage curent at Vg=1.0v,Vds=1.7v

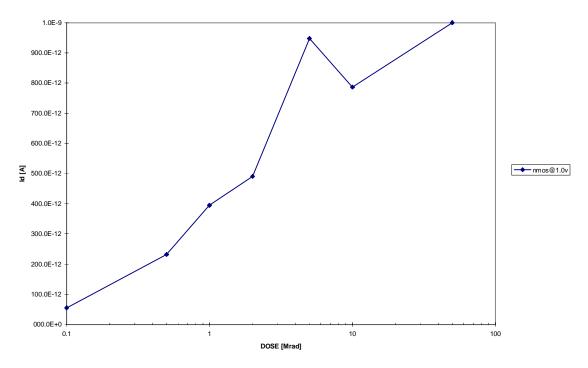


Fig. 11

PMOS [10000/2] leakage current at Vg=-0.8v, Vds=-1.7v

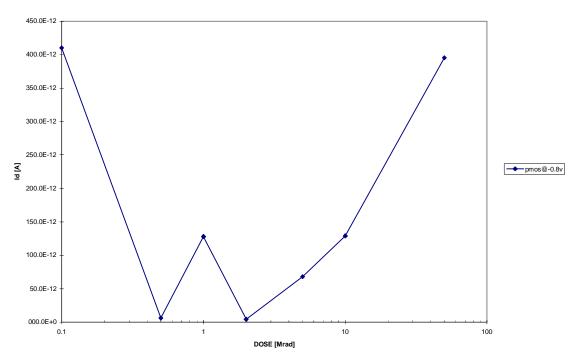


Fig. 12

The Id-Vds curves for the two large mosfets are given in Fig 13 and Fig 14.

NMOS 10000/2 : Id- Vds due to Irradiation

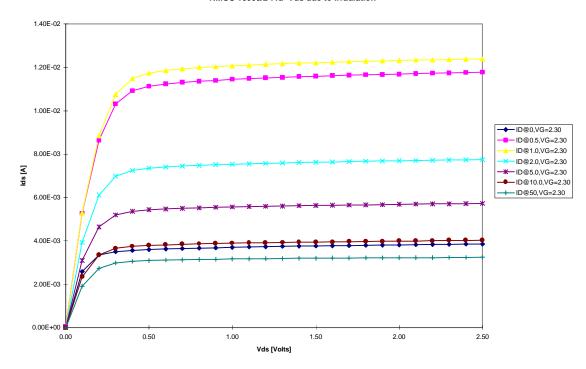


Fig. 13

PMOS 10000/2 Id-Vds due to Irradiation

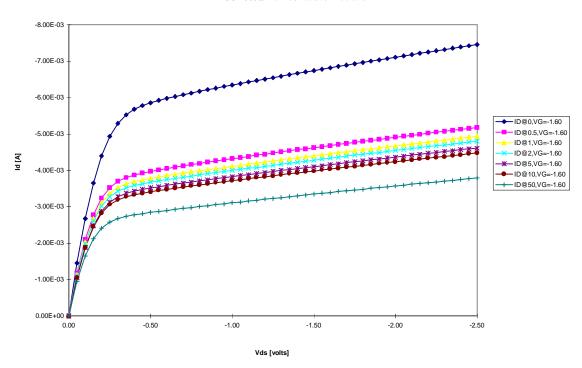


Fig. 14

5. Results on the GEM IPC circuits:

The following data and graphs depict the behavior of the GEM IPC integrated circuits due to Irradiation. The parameters presented here are the output amplitude of the shaped pulse, the gain of the channel and the shaping time for a 30fC input charge (through an 1pF injection capacitor). It is observed that there was a larger amount of variation on output amplitude for the first radiation step totaling 0.5Mrad. Output voltage changed appreciably by 16% and Shaping time by 2.2% for the initial step. For the intended total dose (2 Mrad) that will be seen by the IC the change was 30% and 8% for the output voltage and shaping time respectively. The shaping time for a total dose of 50.0 Mrad changes by 2.7% which is good figure of merit on the shaping time.

Total DOSE in Mrad	Output Amplitude in mV	Gain in mV/fC	Shaping time in nanoSecs
Pre Radiation	98.27	3.27	27.55
0.5	82.16	2.73	28.17
1.0	76.64	2.55	28.91
2.0	69.57	2.31	29.83
5.0	61.25	2.04	31.42
10.0	57.31	1.91	32.20
50.0	47.14	1.57	35.08

GEM IPC output for 30fC input charge

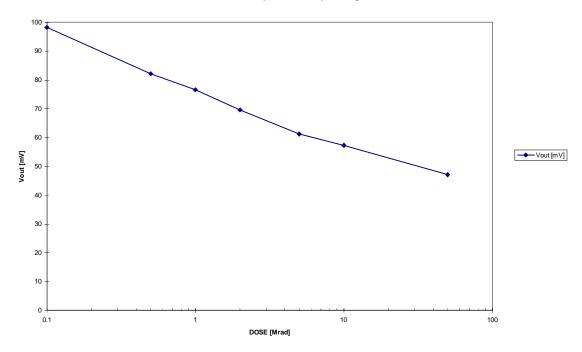


Fig. 15

GEM IPC Shaping time for 30fC input charge

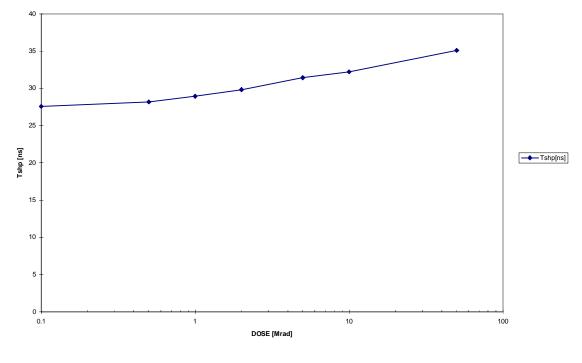


Fig. 16

The following graphs in Fig.17 and Fig.18 depict the variation of output amplitude and shaping time due to various detector capacitance's on irradiation.

IPC-H1 Output vs Detector capacitance

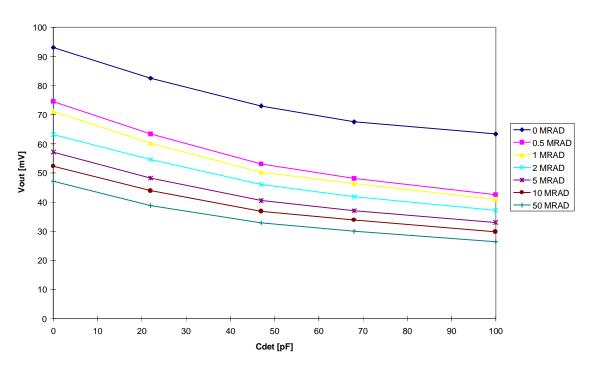
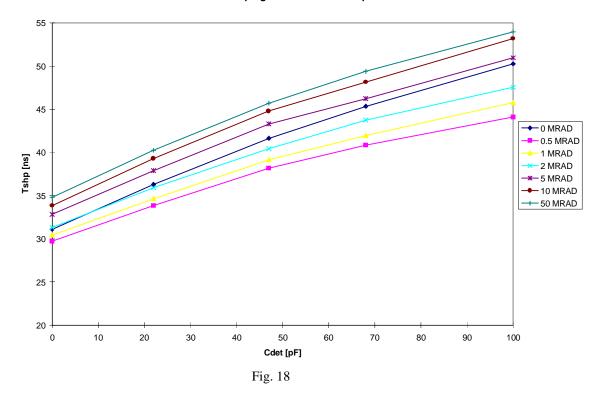


Fig. 17

IPC-H1 Shaping time vs Detector capacitance



Noise performance of the GEM IPC integrated circuit:

Noise measurements were done on the GEM IPC IC's. It is observed that the ENC0 changes by 30% and the noise slope changes by 28% for a total dose of 2.0 Mrad, which will be the total dose that the chip is intended to receive during operation. The total change observed for a total dose of 50.0 Mrad is 86% and 63% for ENC0 and noise slope respectively.

Noise measurements were made for the full channel including the bonding pads and input protection devices having capacitance around 3pf and wiring and printed circuit trace capacitance around 2pf. As mentioned in the design memorandum the noise is dominated by the input transistor and the rest of the major contributors to the noise are the resistors of the high pass circuits, feedback resistors and the input transistors of the first shaper stage.

The Graphs for the ENC0 and Noise Slope are given in Fig. 19 and Fig. 20 respectively in the following page.

GEM IPC ENC0 due to Irradiation

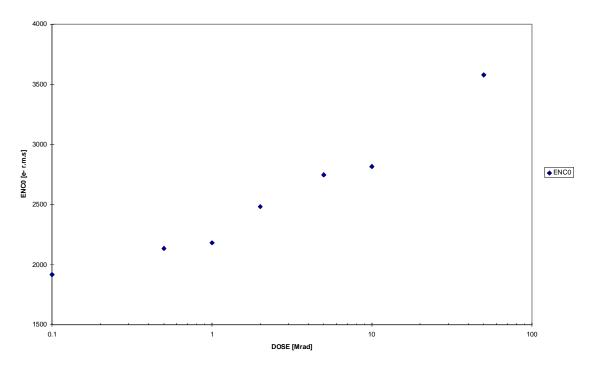


Fig. 19

GEM IPC Noise Slope due to Irradiation

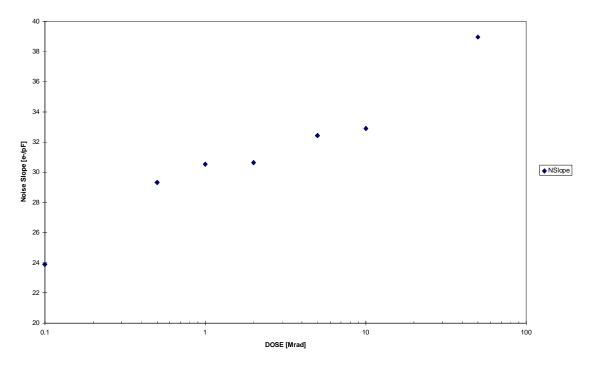


Fig. 20

The output waveform of the GEM IPC preamp/shaper is shown in figure 21. The waveform shown here is for a charge of 30fC and no detector capacitance.

The variation of the peaking time measured as the time taken for the signal to reach its peak (minimum value in this case) from the time the input signal is applied. The variation of peaking time is observed to be 50% change for a total dose of 50 Mrad and 15% for a total dose of 2 Mrad. The peaking time variation is shown if fig 22.

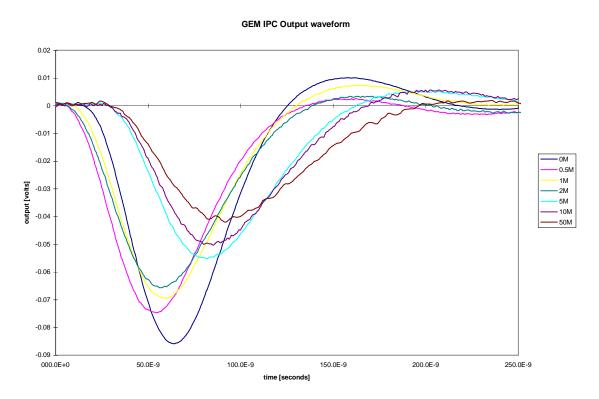
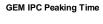


Fig. 21



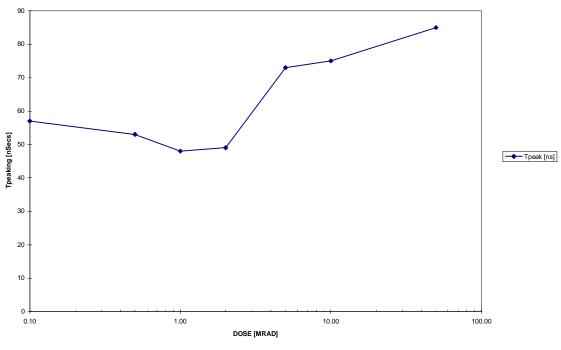


Fig. 22

The GEM IPC IC's were tested for its linearity over the input charge range from 20fC to 150fC.

GEM IPC output linearity [20fc to 150fc]

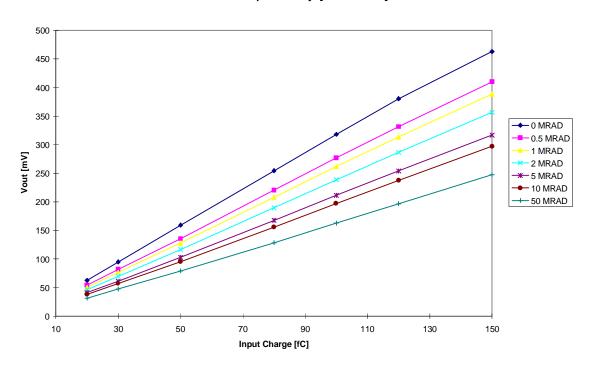
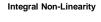


Fig. 23



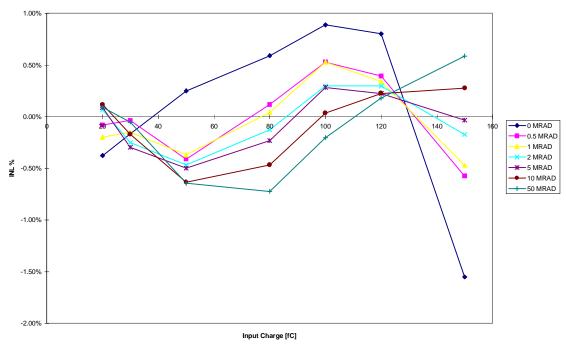


Fig. 24

Figure. 23 illustrates the GEM IPC's input charge vs. output voltage curves and fig 24 illustrates the integral non-linearity of the preamp/shaper chain over the period of radiation.

6. Conclusion:

The observed results of the Irradiation study on the GEM IPC integrated circuit's electronics are summarized as follows.

The results of the test transistors give a picture on the behavior of the mosfets fabricated by this AVSI1-RA process up to the total dose it was irradiated. The P-channel mosfets after its initial disturbance from its behavior, maintained its behavior for successive dose levels, whereas the N-channel mosfets experienced "the rebound" effect on its threshold. It can also be added that this process can be used for digital circuits, since one of the major cause of logic failure being due to the VTNZ effect is not observed in the n-mosfet.

The results on the GEM IPC electronics indicate that up to the intended level of total dose (2 M Rad), which the electronics will receive while operating is as follows. The output amplitude variation of 30% is observed. The peaking time varies by 14% and the noise (ENC) varies by 28%. The shaping time (10%-90%) of the shaper alone varies by 8%. An 43% variation seen by the peaking time for a total dose of 50 Mrad is mainly contributed by the fall time of the preamplifier.

References:

- [1]. GEM IPC Preamp/Shaper design memorandum, Paul. O' Connor, Instrumentation, Brookhaven National Laboratory, NY. BNL -Memo 1992.
- [2]. The Handbook of Radiation Effects, compiled by Andrew Holmes-Siedle and Len Adams, Oxford University Press, 1993